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A Novel and Reliable High accurate High lineaer Very low power and High speed Continuous-time Common-Mode Feedback Circuit in 0.18μm CMOS

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***Abstract*— a new method to design continuous-time Common-Mode Feedback Block (CMFB) circuit is presented in this paper. The most challenges in the proposed idea are to increase the speed and linearity, decrease the settling time error and improve the output swing of the common-mode feedback circuit. Therefore, by applying the worst case simulation (initial condition 0 and 1.8 volts) on the proposed CMFB circuit, the output voltage can be settled in the desired level just after 1.66ns. Moreover, the proposed CMFB has a wide dynamic range voltage to set the output in the preferred value as well. Meanwhile, as MATLAB simulation result demonstrates that by applying the reference voltage (Vref) from 0.55 to 1.35 volts the suggested circuit be able to adjust the output value in the suitable level with low error properly. Furthermore, the mentioned structure is a good choice for low voltage application too. The power consumption of the proposed common-mode feedback circuit is just 123μW with the power supply of 1.8 volts, and 0.5pF capacitor load is applied at the output nodes of the amplifier. Finally, the proposed circuit is simulated in whole process corner and different temperatures in the region from -45℃ to +110℃. Simulation results are performed using the HSPICE BSIM3 model of a 0.18μm CMOS technology and MATLAB software.**

Keywords*— amplifier; Common-mode feedback; low voltage; folded cascode; high speed; Monte Carlo

I. INTRODUCTION

Fully differential amplifiers (FDAs) are used extensively due to their wide output swing, even-order harmonic elimination, large SNR, and stoutness against supply and common- mode (CM) noise compared with their single-ended counterparts. In FDAs, common-mode feedback (CMFB) circuits are required to guarantee proper purpose [9, 10]. Common-mode feedback block (CMFB) is a fundamental circuitry for a fully differential system. Without CMFB, the transistors in the system may easily drift away from saturation region due to mismatch and other process tolerances and cause a system malfunction, especially in low supply voltage applications where the voltage headroom to keep transistors in the saturation region is very small[6]. A CMFB circuit is a network to sense the common-mode voltage, relate it with an appropriate reference, and to feedback the correct common-mode signal with the purpose to cancel the output common-mode current component and to fix the DC outputs to the desired level [1, 4]. Perfectly, the CMFB circuit should only response to CM voltage changes but not differential voltage changes; otherwise, the output dynamic range and linearity of the FDAs would be degraded [9]. Formerly, the most differential-mode circuits have been realized with voltage-mode circuits, where differential nodes in the signal paths have low impedance. In this case, the impedances of the common-mode circuits have negligible effects on the node impedance. Since low node impedance does not introduce low-frequency poles, stability problems are not an issue for designing CMFB's for voltage-mode systems [4]. Modern advances in current-mode signal processing have confirmed that continuous-time current-mode circuits are good alternatives for high-speed signal processing. However, continuous-time differential current-mode circuits introduce unique requirements for common-mode feedback circuits [5]. Since differential nodes in current-mode circuits normally have high impedances, the impedance of the CMFB may have a significant effect on the node impedance. Variation in the node impedances in current- mode circuits usually results in changes

function, which impacts the system performance. Stability problems may also occur. If the CMFB itself has another low-frequency pole, this CMFB circuit may be unstable. Accordingly, common-mode feedback current-mode circuits must satisfy the requirements of very high input and output impedances and stable response [1, 8]. In this paper a new method to design continuous-time Common-Mode Feedback

Block (CMFB) circuit is presented. Moreover, the most focused in the proposed idea are to increase the speed, decrease the settling time error and improve the output swing and linearity of the common-mode feedback circuit. In addition to, by using this method the stability problems are decreased since a low node impedance does not introduce low-frequency poles. Besides, it is a proper choice for using low voltage applications too. The proposed paper is organized as follow: in section II different types of the CMFB are discussed. Proposed common-mode feedback is presented in section III. In section IV simulation results of the paper are specified and finally section V concludes the paper.

II. DIFFERENT TYPES OF THE CMFB

Three different types of CMFB circuits have been developed:

Resistor averaging circuit(R-C), switched-capacitor averaging circuit, and differential difference amplifier (DDA) [8, 9]. First, the resistor-averaging technique achieves very good common- mode (CM) detection accuracy but suffers from large chip area due to the large resistors. Likewise, the R-C common-mode feedback circuit can work at different supplies, but requires large resistance to maintain the high DC gain and large output swing. Second, the switched capacitor CMFB circuit eliminates the resistive loading issue, but, it suffers from clock-injected noise and its application is limited to sampled data systems. Also, it has the smaller passive area, but its loop bandwidth and stability are very sensitive to the supply voltage because of the supply-dependent on-resistance of the switches. [2,12]. The DDA CMFB circuit utilizes transistors to average and compare the CM voltages, the continuous-time operation is hence achieved and the bandwidth of the CMFB circuit can be designed to be close to the bandwidth of the Fully Differential Amplifier with realistic area and power consumption [8,5]. Moreover, it does not need large area passive components, but it has limited linear signal range for the main amplifier and is not suitable for a low supply. However, the conventional DDA CMFB techniques had limited input range and low detection accuracy when the differential input voltage is large, meanwhile, Fig. 1, shows the conventional DDA CMFB circuit. [2]. In order to overcome some of the mentioned drawbacks, a new fast, low settling time error, high linear and low power consumption continuous time common mode feedback is presented the next section.

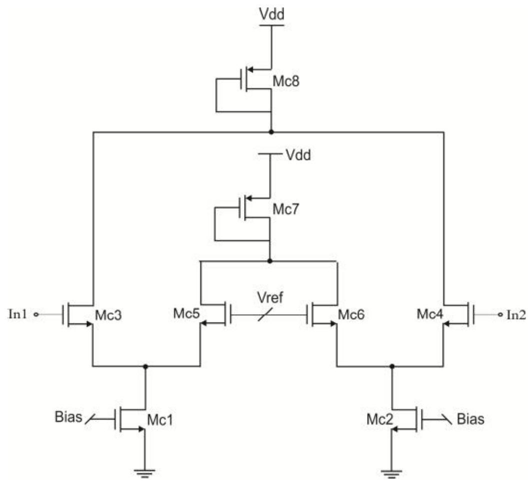

Fig.3. A conventional DDA CMFB circuit

III. THE PROPOSED COMMON-MODE FEED BACK BLOCK

The schematic of the proposed common-mode feedback is depicted in Fig. 2. In the proposed CMFB circuit, the basic idea is to eliminate the diode-connected transistors in the conventional DDA CMFB which applies the error correction signal to the folded cascode op-amp. Since the diode-connected path. As a result, by removing this transistor, the speed of the CMFB circuit will be increased extremely [5]. Therefore, a new simple and reliable CMFB circuit is presented in this paper in order to enhance the linearity, speed, and precision of the conventional differential difference amplifier CMFB circuit. Meanwhile, the PMOS differential pairs of M1 and M2 can play the function of the sensors and actuators of the proposed CMFB respectively, in order to sense the output voltage of the differential amplifiers and set it's value in the desired level as well. Also, the transistors M5-M8 are the current source of the CMFB. In addition to, for improving the linearity of the proposed circuit two resistors (Rs1 and Rs2) are exerted in the source terminals of the differential pair transistors simply. In the meantime, in order to compare the output value of the differential amplifiers with the preferred value, the reference voltage (Vref=Vdd/2) is applied on M3 and M4 properly. On the other hand, it is noteworthy that, by utilizing the PMOS transistors in the proposed CMFB, it is relaxed to remove the contacts in the mentioned nodes (A and B) of the folded cascode amplifier. Fig. 3 shows the simple folded cascode amplifier. Due to that, the nodes capacitors are decreased, also the speed of the CMFB is increased too. Since, as it is clear that, by eliminating the contacts between two nodes, it is possible to merge the mentioned nodes in the layout design. So the parasitic capacitors are reduced and the speed of the circuit is increased as well. Also, it is notable that, a low node impedance does not introduce low-frequency poles. Due to that, in this circuit by applying the actuators output of the CMFB to the NMOS nodes (outc1 and outc2) instead of PMOS nodes (A and B) of the folded cascode amplifier, the stability problems may doesn't occur in the system.

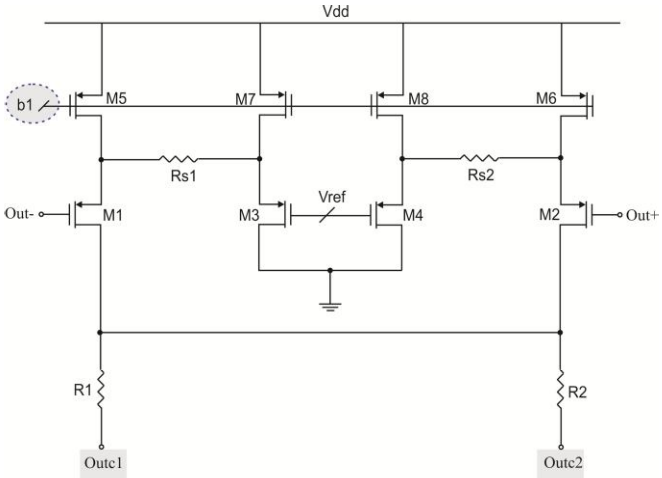

Fig.2 The proposed CMFB circuit

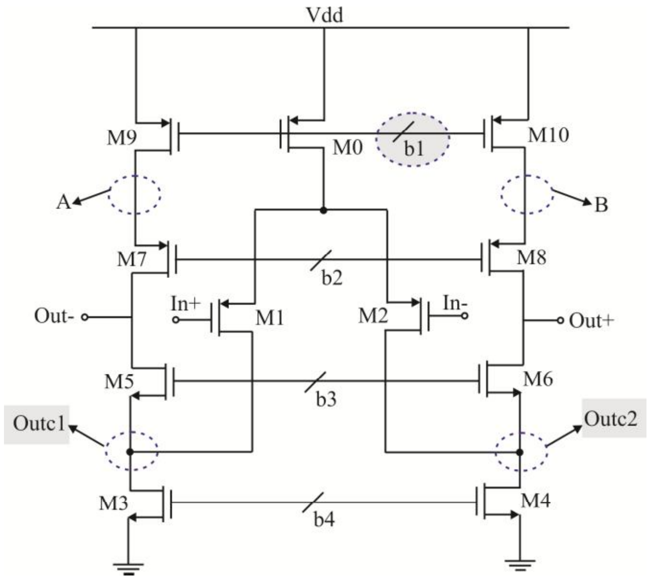

Fig.3 A simple folded cascode amplifier

The another important point is hear, as (2) shows the output swing of the proposed CMFB is improved rather than conventional one. Likewise, the output swing voltages in the conventional and proposed CMFB are presented in (1) and (2) respectively, where ΔV, I and Vth are overdrive voltage, output current and the threshold voltage of the transistor correspondingly. Equation (2) shows, by using this method, the threshold voltage and one overdrive voltage of the (1) is removed as well. Due to this fact, the proposed idea is appropriate option for low voltage applications too, because it needs just fewer voltage to start its performance. Furthermore, the another key feature of the mentioned CMFB circuit is widely dynamic range voltage with low error, it means that if Vref adjusted near to 0.6 to 1.35 volt, the output voltage of the main circuit can be settled in the desired level, owing to that, the voltage of the output nodes is remained near to preferred amount as well. Also, all of the transistors operates in the saturation region.

$$\text{Output Swing}=V_{dd}-3\Delta V-V_{th} \quad (1)$$

$$\text{Output Swing}=V_{dd}-(R1*I)- \quad (2)$$

IV. SIMULATION RESULTS

The simulation results of the proposed circuit are presented in this section. Fig. 4 indicates the transient response of the output common-mode voltage, as it is clear that in the fig. 4, by applying the worst case simulation (initial condition 0 and 1.8 volts) on the proposed CMFB circuit, the output voltage can be settled in the desired level just after 1.66ns. Also, Monte Carlo simulation results are applied to the transient response of the output common-mode voltage for 3% variation of transistors threshold voltage and temperature variation on the proposed CMFB which are shown in fig. 5 and 6 respectively. Simulation results verify that even with these possible variations proposed circuit offers estimated performance. Therefore, as MATLAB simulation result demonstrates the output common-mode voltage error in whole process corner in the fig. 7. As it is clear that, in fig. 7, by applying the reference voltage (Vref) from 0.55 to 1.35 volts, the suggested common-mode voltage be able to keep the output voltage in desired value (low error) properly. Meanwhile, the output Folded cascode amplifier FFT spectrum is depicted in fig. 8. By applying a 49.9MHz sinusoidal input with the amplitude of 1mV results in an output THD less than -57dB. It is noteworthy that by utilizing the proposed CMFB the linearity of the amplifier is improved well. Finally, the layout of the suggested CMFB circuit is shown in fig. 9. It is notable that, the circuit has been designed in a typical 0.18 µm CMOS process with a power supply of 1.8V and simulated by HSPICE software using level 49 parameters (BSIM3v3) and MATLAB software.

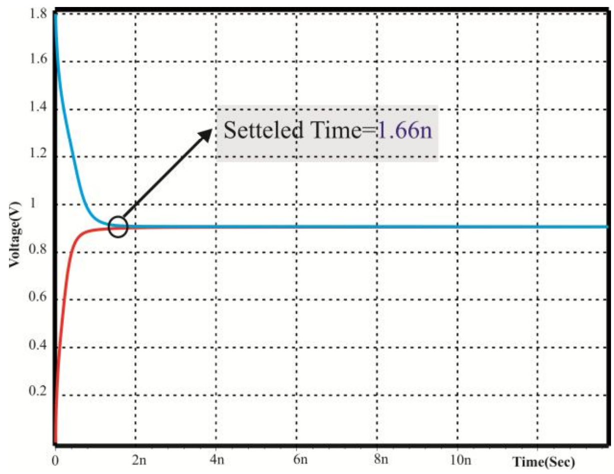

Fig.4 Transient response of the output common-mode voltage

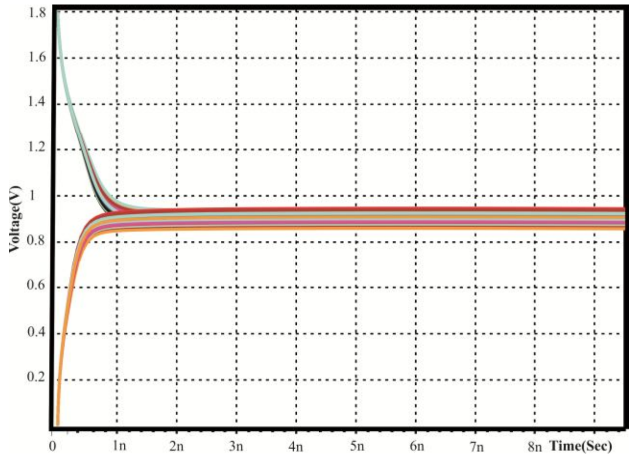

Fig.5 Transient response of the output common-mode voltage by applying 3%varation of transistors threshold voltage

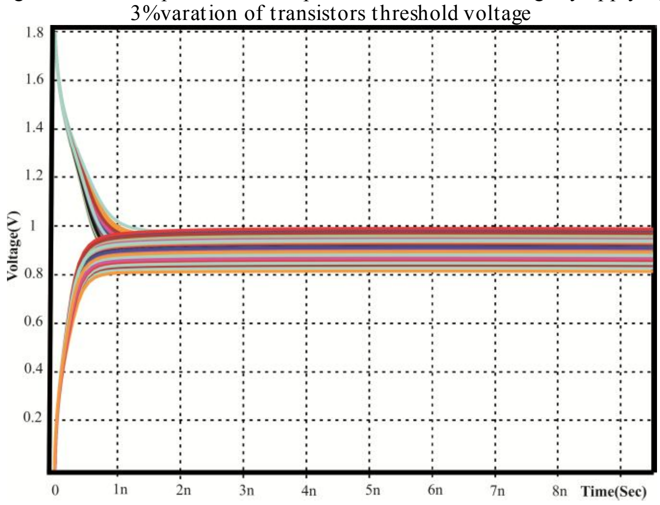

Fig.6 Transient response of the output common-mode voltage by applying temperature variation from -45 to +110℃

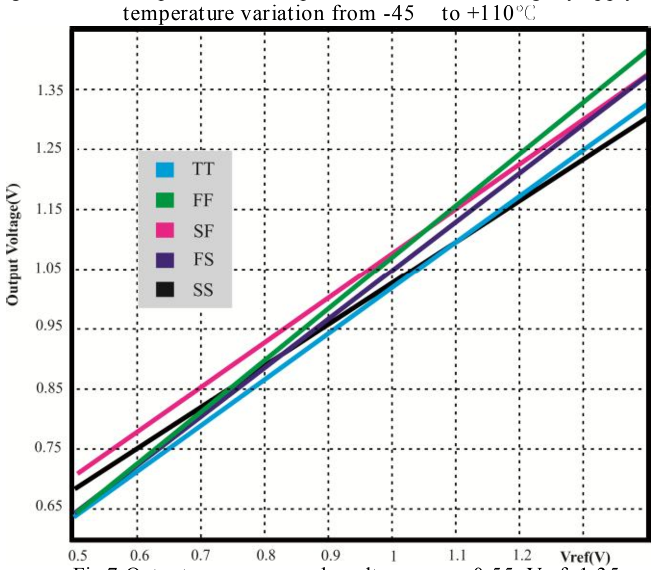

Fig.7 Output common-mode voltage error: 0.55<Vref<1.35

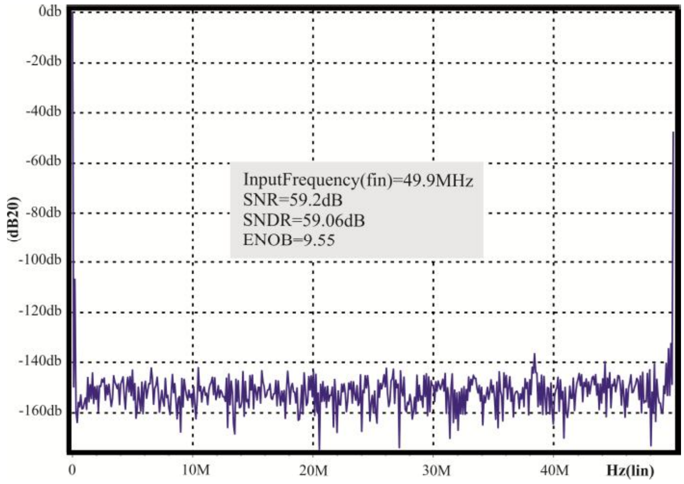

Fig.8 Output FFT spectrum of the folded cascode amplifier

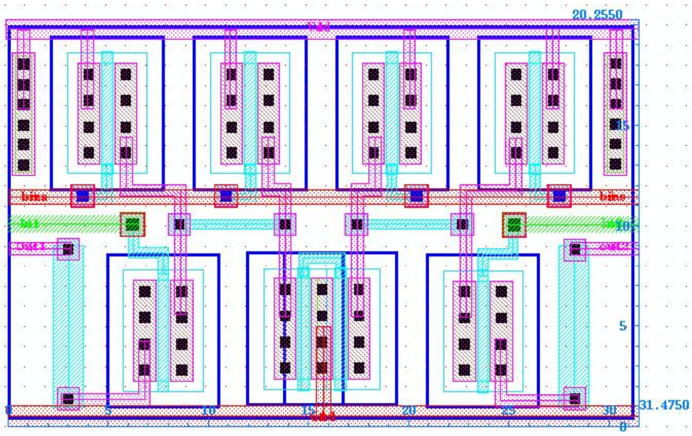

Fig.9 Layout of the proposed CMFB

V. CONCLOUSION

In the proposed paper a new simple and reliable technique to design a continuous-time common-mode feedback circuit is presented. The main aim of the proposed idea are decreasing the output settling time error, increasing the speed, improving the linearity and output swing of the common-mode feedback circuit. Besides, the proposed CMFB circuit has an extensive dynamic rang voltage to set the output in the desired value too. As MATLAB simulation result indicates in whole process corner, the proposed circuit can adjust the output in reliable value by applying the Vref from 0.55 to 1.35 volt suitably. Moreover, the mentioned structure is a proper candidate for low voltage applications too, since it needs just a fewer voltage to starts its performance. The power consumption of the proposed circuit is just 123µW with power supply of 1.8 volt, also table I compare this work with the similar previous one. Simulation results are performed using the HSPICE BSIM3 model of a 0.18µm CMOS technology and MATLAB software.

Table I. Comparison Table

	[5]	[12]	[13]	This work
Technology	0.35µm	0.13µm	0.18µm	0.18µm
Supply Voltage	3.3	1.8V	0.9V	1.8V
Power consumption	-	9mW	-	123µW
Settling error	0.35mV	-	0.9mV	0.1mV
Settling speed	1.1nS	40ns	30ns	1.66nS
Chip area	-	-	-	20.25µm* 31.47µm

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