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A 41MHz 63dB and 1.22mW Variable Gain Amplifier in 0.18µm CMOS

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Abstract **in this paper a new reliable technique to design a high linear, low sensitive, wideband DC gain range and low power variable gain amplifier is presented. Therefore, by applying the proposed idea on the folded cascode amplifier, it is possible to achieve a 63dB DC gain, 41MHz (-3dB) bandwidth, accompanied with high linearity and low sensitivity as well. Also, the power consumption and unity gain bandwidth of the proposed VGA are just 1.22mW with the power supply of 1.8 volts and 4.87GHz respectively, and 1pF capacitor load is applied at the output nodes of the amplifier. Moreover, the proposed structure is simulated in all process corners and different temperatures in the region of -45 to +85 ºC. Simulations are performed for all corner conditions by HSPICE using the BSIM3 model of the 0.18µm CMOS technology and MATLAB software.**

Keywords *variable gain amplifier; low power; low voltage; folded cascode; amplifier; DC gain*

I. INTRODUCTION

One of the most significant building blocks of analog ICs is a variable gain amplifier (VGA), which is utilized in many applications in order to stabilize the voltage amplitude of a signal at its output [1]. Therefore, the VGA is usually employed in an automatic gain control (AGC) circuit to maximize the dynamic range of systems such as medical hearing aid equipment, wireless transceiver designs and communication systems, etc.[2,3]. Moreover, Gain of the VGA can be controlled either digitally or continuously [1-4]. The disadvantage of the digital approach lies in a discrete gain variation that causes a non-continuous control of the output signal [3, 6]. Also, the digital approach can have a relatively larger gain range with smaller gain error but it is difficult to achieve small gain steps due to the limited number of control bits. Inversely, VGAs based on the analog control can control gain continuously, although the gain error may be larger than digital approach counterpart, but it represents a better choice for AGC circuits [2, 5, 6, and 8]. Though the specifications of a VGA can differ significantly in terms of power consumption, bandwidth, linearity, noise and for different applications, common specifications of the VGA are to provide a reasonable gain range with an accurate dB-linear characteristic [6-9]. In this paper a new reliable method to design a high linear, low sensitive, wideband DC gain range and low power variable gain amplifier is presented. The proposed paper is organized as follows: in section II; different types of differential amplifiers are specified. in section III; Proposed VGA is presented. Simulation results are conferred in section IV and finally, section V concludes the paper.

II. FULLY DIFFERENTIAL AMPLIFIERS

Most modern devices such as high-speed analog-to-digital converters require using high-speed Operational Amplifier (op amp) [10]. Generally, ooperational amplifiers are used in analog building blocks and analog-mixed signal systems. The requirement for high density, low cost, and low power dissipation of high precision VLSI systems demands high-performance analog circuits [10-12]. Also, they are mainly classified into single ended output and differential-ended output operational Amplifiers [11]. The fully differential operational amplifiers have several advantages over single-ended output op-amps, such as stable input common mode voltage, reduction of harmonic distortion, doubling of output voltage swing, and suppression of coupled noise due to substrate and power lines [11, 13]. In order to achieve high DC gain and proper bandwidth, telescopic cascode and folded cascode structures are two known examples [16]. The telescopic architecture is a good candidate for a low noise, low power, and high gain OTA [13]. The performance of simple telescopic OTA is limited by its input and output voltage swing. However, it provides high gain as well as high speed [13, 14, and 16]. As a result, this structure is not an option for systems with low supply voltages. On the other hand, in low voltage CMOS process, folded cascode amplifier is one of the most favorite architectures for both single stage and the multi-stage amplifiers due to its high gain and reasonably large output signal swing. [13,17]. Moreover, in the folded cascode amplifier, the differential PMOS input pair is chosen over its NMOS counterpart, due to its higher non-dominant poles, lower input common mode range and lower flicker noise [15-17].

III. THE PROPOSED COMMON-MODE FEED BACK BLOCK

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The proposed variable gain amplifier circuit is depicted in Fig.6. In the proposed circuitry the differential pairs of M1-M2 and M11-M12 are the Transconductance stage (input stage) where M3-M6 and M7-M10 are the cascode transistors of the folded cascode amplifier. The main purpose of the proposed structure is to achieve a wideband dynamic DC gain range and proper -3dB bandwidth with low power consumption and high linearity. Equation (1), shows the DC gain of the amplifier conventionally, where Av, Gm and Rout are the DC gain, transconductanse and output resistance of the amplifier respectively. In this circuit by varying the output resistance and transconductance consequently, the DC gain of the amplifier will be changed. Therefore, the output resistance and transconductance of the amplifier are controlled by external voltage (Vc) which is applied to the current source transistors Ma1and Ma2. As a result, by changing the Vc, the DC gain will be changed too. On the other hand, by adjusting the Vc to the lowest and highest voltage, the minimum and maximum DC gain is attained respectively. Meanwhile, for improving the linearity of the amplifier, the resistance of the Rs is applied to the source terminals of the input differential pair transistors simply. As discussed above, by adding the resistor into source terminals of the input differential pair, the linearity and susceptibility of the circuit is increased and decreased respectively. Owing to that, the DC gain is not dependent on the bandwidth and Vc extremely. It is noteworthy that, as simulation results show in the section IV, by applying the temperature and process corner variation, and Monte-Carlo simulation, the operation of the proposed VGA is almost constant in most condition. Thus, its lower sensitivity makes it a reliable choice for the most applications. Consequently, the proposed circuit provides features like the wide gain range with high linearity, suitable bandwidth, and possibility to reach both positive and negative gain altogether.

$$Av=Gm*Rout \qquad (1)$$

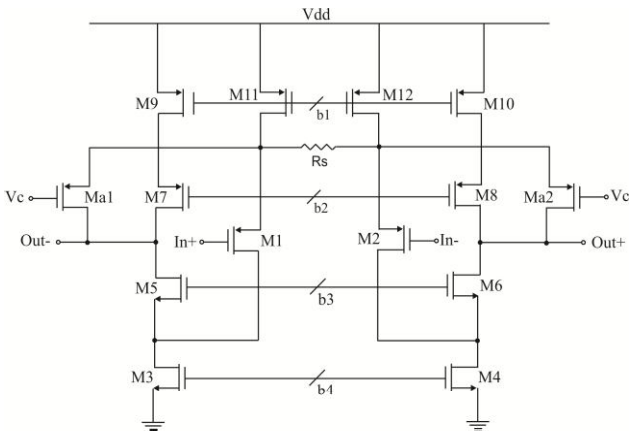

Fig.1 The proposed VGA circuit

IV. Simulation Results

In this section, simulation results of the proposed variable gain amplifier are presented. Fig. 2 and fig. 3 indicate the ac simulation of the proposed VGA structure for getting maximum and minimum DC Gain respectively. In the meantime, in the fig. 2, -3dB Bandwidth (MHz) is presented in all process corners too. Unity gain bandwidth of the amplifier is shown in fig. 4. Also, the diagrams of the fig. 5 and fig. 6 demonstrate the relation of DC gain (Av) versus Vc and temperature which are drawn by using MATLAB software separately. The Monte Carlo simulation results are applied to the DC gain of the proposed VGA for 2% variation of the transistors threshold voltage which is shown in fig. 7. As it is clear in the fig. 7, by applying the Monte Carlo simulation on the circuit, the DC gain will be achieved almost 60dB as well. Meanwhile, the output FFT spectrum of the proposed VGA is depicted in fig. 8. By applying a 49.9MHz sinusoidal input with the amplitude of 1mV, the output THD will be less than -71dB. The layout of the suggested VGA circuit is shown in fig. 9. The circuit has been designed in a typical 0.18 CMOS process with a power supply of 1.8V and simulated by HSPICE software using level 49 parameters and MATLAB software.

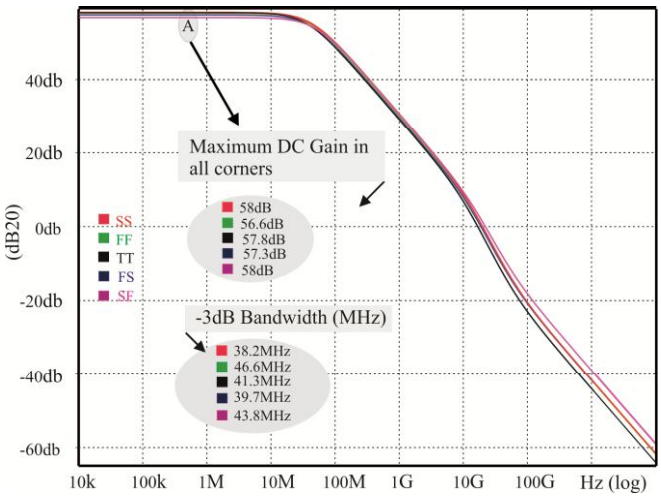

Fig.2 Ac simulation for maximum gain in all corners

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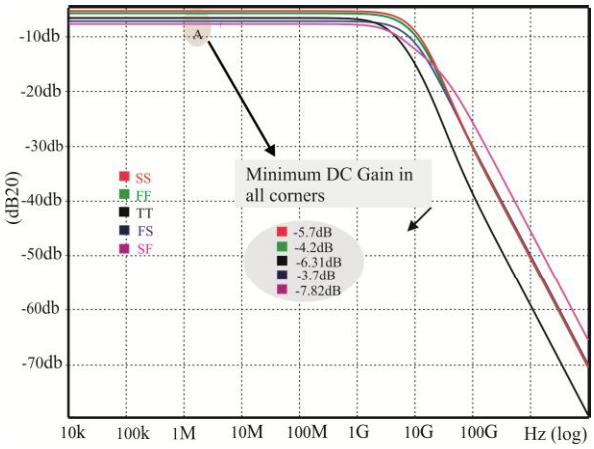

Fig.3 Ac simulation for minimum gain in all corners

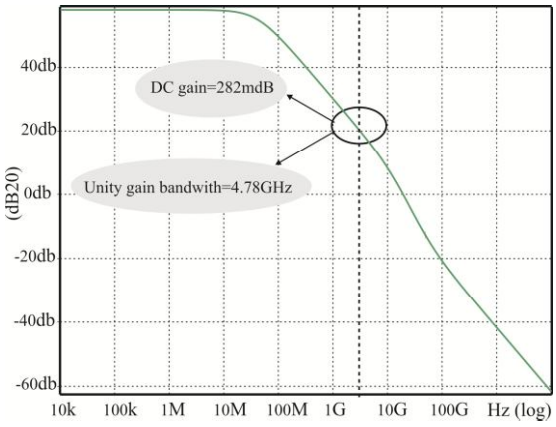

Fig.4 Unity gain bandwidth of the amplifier in TT corner

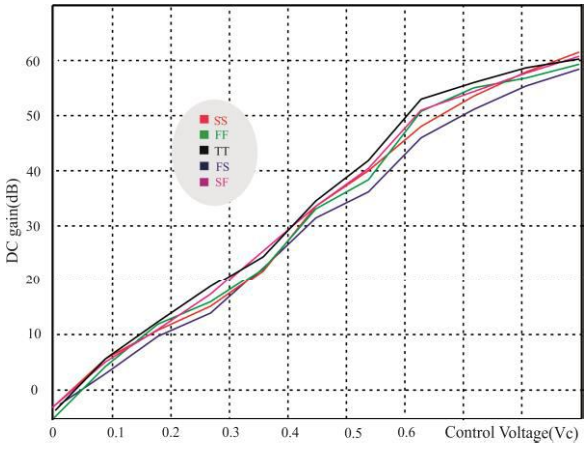

Fig.5 DC gain vs. the Control voltage (Vc) in all corners

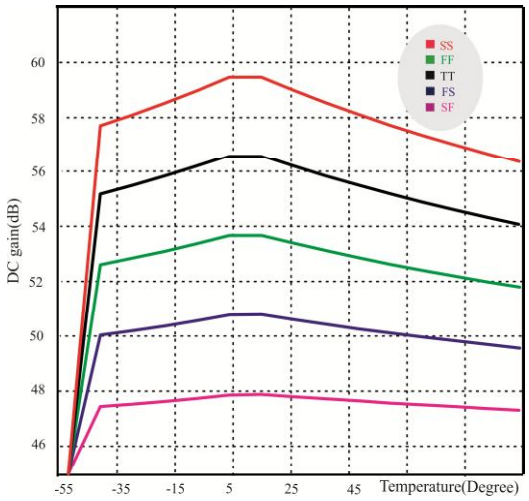

Fig.6 DC gain vs. Temperature in all corners

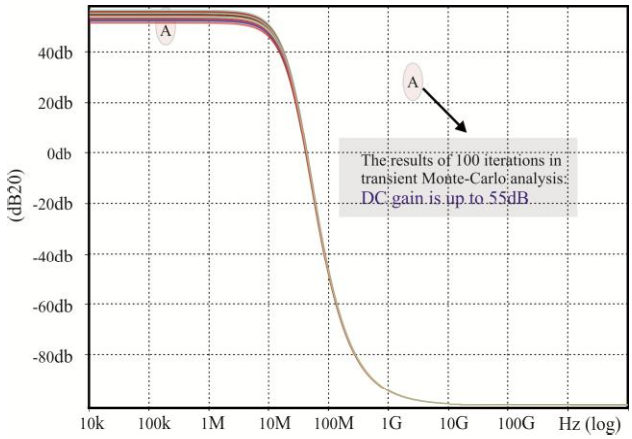

Fig.7 DC gain of the proposed VGA by applying 2%varation of the transistors threshold voltage

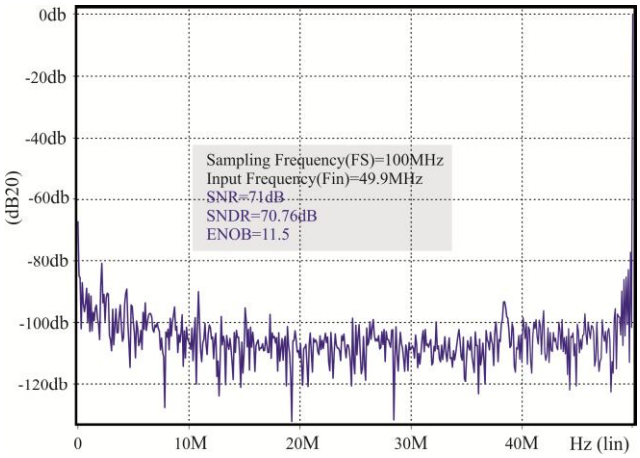

Fig.8 Output FFT spectrum of the proposed VGA

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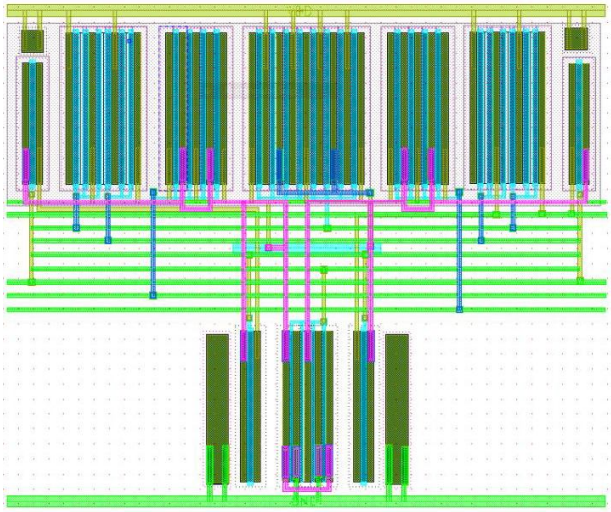

Fig.9 Layout of the proposed VGA

V. CONCLOUSION

A new simple and reliable method to design a linear, low sensitive, wideband DC gain range and low power variable gain amplifier is presented. Therefore, by applying a proposed idea on the folded cascode amplifier, it is possible to achieve a 63dB DC gain, 41MHz (-3dB) bandwidth, accompanied with high linearity and low sensitivity as well. Also, the power consumption of the proposed VGA is just 1.22mW with the power supply of 1.8 volts, and 1pF capacitor load is applied at the output nodes of the amplifier. Finally, the table I compares this work with similar previous ones. The circuit has been designed in a typical 0.18 CMOS process with a power supply of 1.8V and simulated by HSPICE using level 49 parameters and MATLAB software.

Table I. Comparison Table

	[2]*	[4]	[9]	This work
Technology	0.18 µm	0.18µm	0.18µm	0.18µm
Supply Voltage	3.3V	1.8V	1.8V	1.8V
Power consumption	12mW	-	8.1mW	1.22mW
-3dB bandwidth	18MHz	10.8MHz	0.6-1.6MHz	41.3MHz
Gain range	55dB	50dB	84dB	63.6dB
Unity gain bandwidth	-	-	-	4.78GHz

*Measurement

References

[1] D. Arbet, M. Kováč, L. Nagy, V. Stopjaková, J. Brenku, "LOW-voltage bulk-driven variable gain amplifier in 130 nm CMOS technology," IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), pp. 1–6, 2016

[2] M. El-Shennawy, N. Joram, F. Ellinger, "A 55 dB range gain interpolating variable gain amplifier with improved offset cancellation," IEEE 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), pp. 1-4, 2016

[3] D. Arbet, M. Kováč, L. Nagy, V. Stopjaková, M. Sovčík," Variable-gain amplifier for ultra low voltage applications in 130nm CMOS technology" IEEE 39th International Convention on Information and Communication ,pp. 51-56, 2016

[4] P. Gao, Z. Wang, J. Xu; W. Li, Y. Wu, L. Tang, "A low power variable gain amplifier with 50 dB dynamic range, " IEEE MTT-S International Microwave Workshop Series on Millimetre Wave Wireless Technology and Applications, pp. 1-4, 2012

[5] F. D. Baumgratz, H.Li, S. Bampi, C.E. Saavedra," Wideband low noise variable gain amplifier," IEEE 28th Symposium on Integrated Circuits and Systems Design (SBCCI), pp. 1-6, 2015

[6] Ha. Liu, X. Zhu, C. C. Boon, X. Yi, L. Kong, "A 71 dB 150 um Variable-Gain Amplifier in 0.18um CMOS technology," IEEE Microw. Wirel. Compon. Lett. , Vol.25, pp.334-336, March 2015

[7] T. Sánchez-Rodríguez, J. A. Galán, M. Pedro, A. J. López-Martín, R.G. Carvajal, J. Ramírez-Angulo, "Low-power CMOS variable gain amplifier based on a novel tunable trans conductor" IET Journals & Magazines Circuits, Devices & Systems, Vol. 9, pp.105-110, April 2015

[8] A. Aimone, A. Malignaggi, A. Hamidian, G. Boeck, "Ultra wide band variable gain amplifier for V-band Transceivers," VDE German Microwave Conference (GeMiC), pp. 1-4, 2014

[9] E. Belousov, K. Lomovskaya, "A 84-db wideband low-power variable gain amplifier," IEEE International Symposium on Signals, Circuits and Systems ISSCS, pp. 1-4, 2013

[10] A. V. Kosykh, S. A. Zavyalov, R. R. Fakhrutdinov, K. V. Murasov, R. A. Wolf, "Fully differential high-gain high-GBW operational amplifier in 250 nm BiCMOS process," IEEE 17th International Conference of Young Specialists on Micro/Nanotechnologies and Electron Devices (EDM), pp. 196-200, 2016

[11] Sh. B. Nerurkar, Kh. H. Abed, "CMOS fully differential operational transconductance amplifier design for delta-sigma modulators," IEEE Southeast on, pp. 52-57, 2008

[12] M. Kumngern, F. Khateb, "Fully differential difference transconductance amplifier using FG-MOS transistors," IEEE International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), pp. 337-341, 2015

[13] S. A. Enche, Ab. Rahim, M. A. Ismail, A. I. Abdul Rahim, M. R Yahya, A. F. A. Mat, "A wide gain-bandwidth CMOS fully-differential folded cascode amplifier," IEEE International Conference on Electronic Devices, Systems and Applications, pp. 165-168, 2010

[14] P. Patra, S. Kumaravel, B. Venkatramani, "An enhanced fully differential recycle folded cascode OTA," IEEE International Multi-Conference on Systems, Signals & Devices, pp. 1-5, 2012

[15]. F. A Matter, M.F Ibrahim, Kh. A Shehata, "CMOS single stage fully differential telescopic cascode OTA with gainboosted technique on Information Technology and Computer Applications (WCITCA), pp. 1-6, 2015

www.irantract.com

[16]. K. Gulati and Ha. Lee, Fellow, IEEE "A High-Swing CMOS Telescopic Operational Amplifier," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 33, NO. 12, DECEMBER 1998

[17]. S. Sharma, P. Kaur, T. Singh, M. Kumar, "A Review of Different

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