3rd International Conference on Knowledge-Based Engineering and Innovation (KBEI-2016)
Dec. 30th, 2016
(Tehran Provine Payame Noor University) – Tehran, Iran

Design of High Speed and low power D Flip-Flop by CNTFET Technology

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***Abstract*— Flip-flops are widely used to receive and maintain data in selected sequences during recurring clock intervals for a limited period of time sufficient for other circuits within a system. So increasing the speed and decreasing power of the flip-flops caused to increase the total speed and decrease power of the circuits. This paper purpose is twofold, High-Speed and low power design of D flip-flop using Carbon Nano Tube Field Effect Transistors (CNTFETs). The proposed designs were simulated using HSPICE simulator with 32nm Stanford CNTFET model. simulation results is based upon 1 volt power supply voltage and operating frequency at 1 GHZ, the proposed designs is 44% faster and consumes 29% less power compared with recent existing conventional CNTFET based D flip-flop circuits.**

Keywords- CNT; CNTFET; D Flip-Flop; High Speed ; Circuit simulation

I. INTRODUCTION

Today, with advances in technology and reducing the size of transistors in nano dimension, have accumulated billions of transistors on a chip. While there are limits for removing excess heat from power generated from these transistors. Power is one of the primary problems of today's systems, this amount is between 30 to 50 percent of total power consumed by the clock systems like clock Reseller network, flip-flops and Latches.

Also due to the increasing use of portable devices with limited battery life, is required to the low power consumption, space, and high efficiency circuits. The main priority in these devices are durability of battery life. Therefore, design of high-speed circuit and low power consumption is particularly important. Due to these reasons, reducing power and increasing speed of flip-flops can improve the overall speed and power consumption of the circuit.

Technology limitations of Mosfet technology, as well as the growing technology in recent years in the fields of nanotechnology, nano-electronics in particular have increased considerably. Carbon nanotubes, due to its unique electronic and mechanical properties as a technology, is a rival for current silicon technology[1].

In this paper, two novel designs of D flip-flop device are proposed using CNTFETs as emerging technology. There are many D flip-flop designs like this work, such as[2],[3] and [4]. In this works design a flip-flop gate using CNTFETs technology and they decrease power and delay in comparison with D flip-flops that designed by MOSFET technology flip-flops. In the next sections basics of carbon nanotubes, CNTFETs, d flip-flops and proposed designs are explained.

II. BASICS OF CARBON NANOTUBES

The Carbon nanotubes were discovered by S.Ijiima in 1991 while performing some experiments on molecular structure composed of carbonium. Carbon nanotubes In addition to being lightweight, have higher specific strength than steel and also can be a good alternative to metals or semiconductors. This material, because of its geometric configuration can show conductive or semi-conductive properties and that distinguishes these materials from other similar materials. The most common methods are used for producing nanostructures such as carbon nanotubes, are chemical vapor deposition, arc discharge and laser vaporization. They can be considered as the result of folding graphite layers into carbon cylinders and may be composed of a single shell–single wall nanotubes (SWNTs), or of several shells multi-wall nanotubes (MWNTs) as shown in fig.1[5]. Depending on the folding angle and the diameter, nanotubes can be metallic or semiconducting. To determine how the spin of graphene sheets, for making carbon nanotubes, is used a chiral vector. Based on the chiral vector, the circular vector that is perpendicular to the axis of the tube, CNTs are classified into Arm Chair, Zigzag & Chiral as shown in fig.2 [5]. SWNTs (single wall CNTFET) are typically one atom in wall thickness, few tens of atoms in circumference and many microns in length.

III. CARBON NANO TUBE FIELD EFFECT TRANSISTOR

The importance of the CNT diameter is that it determines the band gap energy of the tube. The following relation expresses the SWCNT(single wall CNT) band gap energy.

$$E_{gap} = \frac{2y_{0c-c}}{d} \quad (1)$$

Where E_{gap} is bandgap, y_0 is the carbon-to-carbon distance (0.142nm) and d is the diameter of the nanotube. As

d gets larger the band gap becomes smaller and the nanotube becomes more conducting. This can be thought as the tube with reduced curvature looking more like planar graphene. Electrical transport inside the CNTs is affected by scattering caused by defects and lattice vibrations that lead to resistance, similar to that in bulk materials. The one dimensional nature of the CNTs and their strong covalent bonding drastically affect the processes. Semiconducting behavior of nanotubes is affected by their chirality's. In a nanotube chirality is the angle difference between the graphene strip's orientation and the axis of the resulting nanotube. Semiconducting behavior of CNT is the main reason for the strive to build CNT Field effect Transistors (CNTFET) (fig.3)[6].

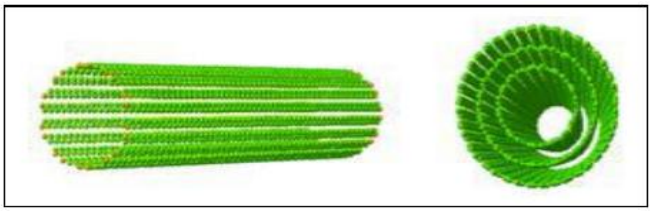

Figure 1. Single walled and multi walled nanotubes[5].

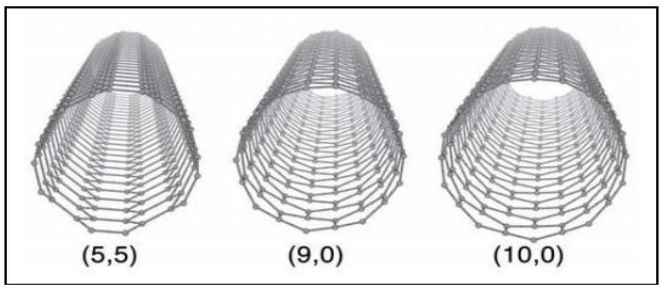

Figure 2. Arm-chair, zigzag and chiral forms of nanotubes[5].

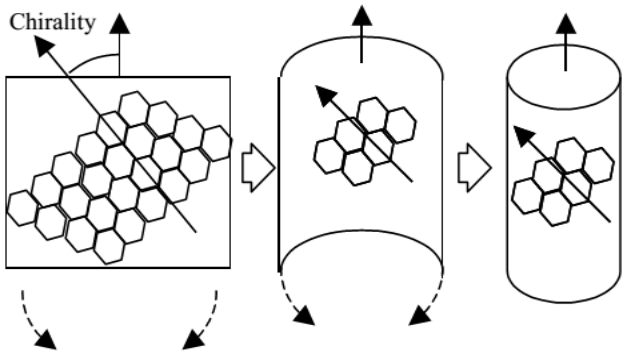

Figure 3. Chirality of a CNT [6].

A CNT can act as a metal or a semiconductor depending on its chirality. A vector (m, n) connecting the centers of the two hexagons is called the chiral vector. If m=n or m-n=3i, where it is an integer, then CNT acts as metal otherwise it acts as a semiconductor. The diameter of the CNT is given by[7]:

$$D_{CNT} = \frac{a\sqrt{3}}{\pi}\sqrt{n^2 + m^2 + nm} \qquad (2)$$

$\alpha = 0.142$ nm, the inter atomic distance between each carbon atom and its neighboring atom. (n, m) are the chirality of the CNT[8].

To design a circuit of best performance with an average power consumption and speed, the important parameter is the threshold voltage because this affects the switching speed, the current and leakage power. In CNTFET, by adjusting the diameter, the threshold voltage can be controlled and is given by [9]:

$$V_{th} \approx \frac{E_g}{2q} = \frac{av_\pi}{\sqrt{3}qD_{CNT}} \qquad (3)$$

Where $a = 2.49A°$ is the carbon to carbon atom distance v_π is the carbon $\pi - \pi$ bond energy in the tight bonding model $q = 1.6\ e^{-19}$ C is the electron charge E_g is the energy gap hence by adjusting the diameter of CNT different transistors with different turn on voltage can be implemented.

There are several types of CNTFETS that have been fabricated. The geometry of the CNTFET may be planar and coaxial as shown in Fig. 4(a), 4(b) [9].

IV. D FLIP-FLOP

Flip flops and latches are bi-stable elements, which generally sample their input data continuously, whenever an enable input occurs or at a particular time instant defined in term of a clock signal Delay flip-flop stores a particular input pattern and allow processing of it by other parts of digital circuit to obtain complex functions. One flip-flop that are used frequently is the conventional positive edge triggered delay flip flop, which Set-Reset NAND gate based latch is used for implementing delay flip flop along with the inverter Din is the input data applied to set input of SR latch and its complement is applied to reset input[10].

Q is the delayed version of Din, acting as the output with Q as the complement of Q is also available[10].

Furthermore flip-flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size of CMOS technology process scaled down according to Moore's Law, designers are able to integrate many numbers of transistors onto the same die. The more transistors there will be more switching and more power dissipated in the form of heat or radiation. Heat is one of the phenomenon packaging challenges in this era. it is one of the main challenges of low power design methodologies and practices.

D flip-flop is considered to be the most essential memory cell in the vast majority of digital circuits, which brings it extensive utilization, especially under current circumstances where high-density pipeline technology is frequently employed in digital integrated circuits and massive flip-flop modules are indispensable components[11].

As a continuous research effort, numerous different types of D flip-flops have been invented, investigated, and the recent research trend has turned to high-speed low-power performance. To implement high performance chip, choosing the most appropriate D flip-flop has obviously become an extremely significant part in the design flow. The reasons come from two aspects: one is that D flip-flop has direct effect on the clock frequency of digital circuit systems, especially for some micro-structures with shallow logical depth; the other one is that D flip-flop is an indispensable component of clock network[11].

V. PROPOSED DESIGNS

In this section, the proposed D flip-flops gates are analyzed and evaluated under various test conditions using HSPICE simulator with Stanford model of 32nm CNTFET that includes real device non idealities with CNT charge screening effects, scattering, parasitic, back gate effect, gate resistances and capacitances. Reference 9 was used to implement these two designs. In order to implement these two designs references 1, 2 and 3 were used, and the results were compared with other similar CNTFET based design. The results shows the proposed D flip-flop are the most efficient D flip-flop with CNTFET technology. First and second proposed circuits are shown in Fig.5 and fig.6.

The transient simulated waveform of the first and second proposed gates are shown in Fig.7 and Fig.8 that verify its correct functionality.

All circuits are simulated at 1GHz operating frequency and at 1V power supply voltage.

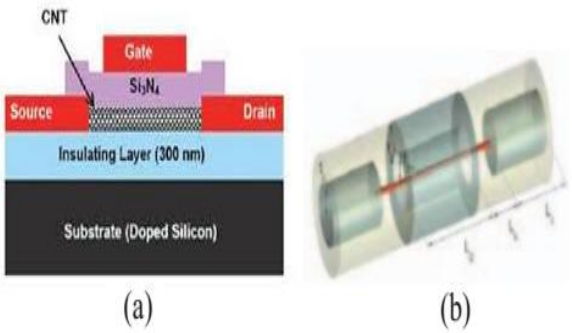

Figure 4. Geometry of CNTFET (a) planar (b) coaxial[9].

The results shows the delay is lower than other design in first design. However design in reference 1 show lower power usage. The second design shows lower delay and lower power usage among all the other designs(Table 1 , fig.9 and fig.10).

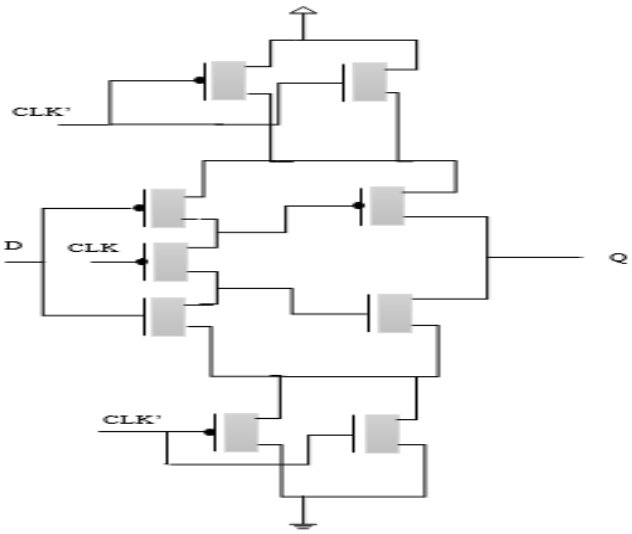

Figure 5. First proposed design.

Table II shows the simulation results of proposed designs at different operating frequency and at 1V power supply voltage.

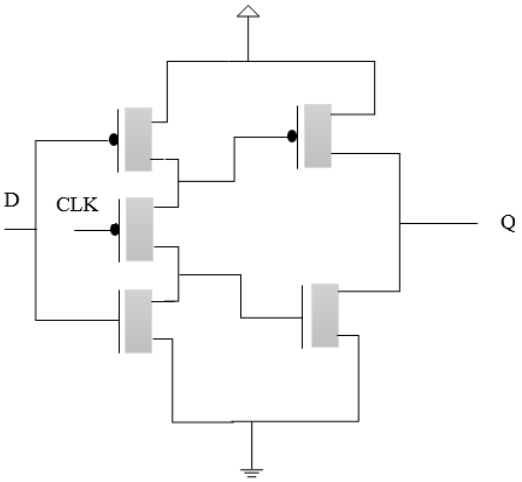

Figure 6. Second proposed design.

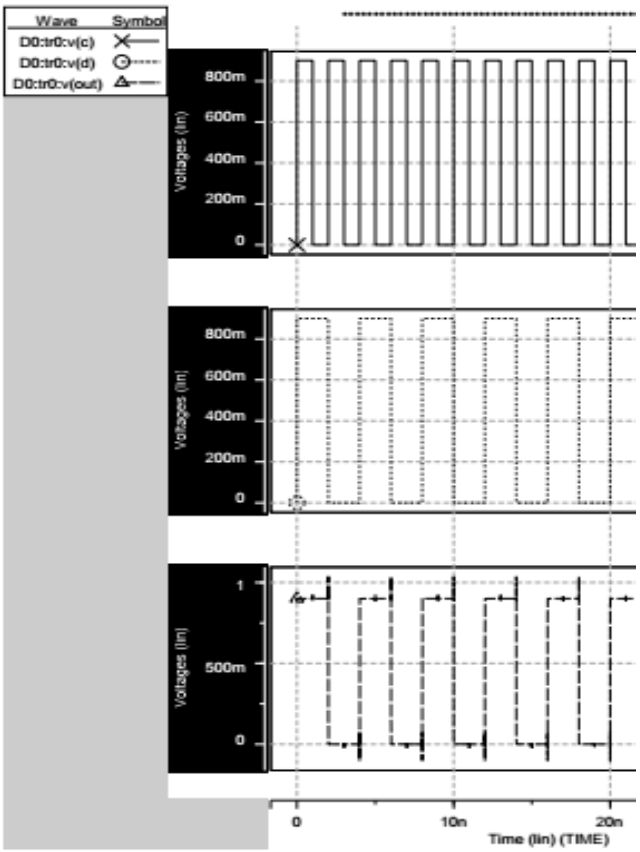

Figure 7. Transient simulated waveforms of First proposed design.

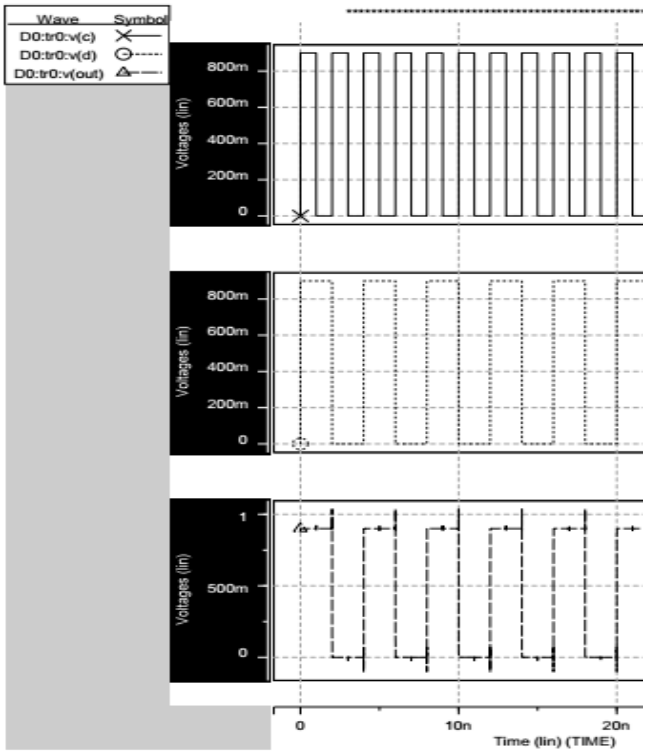

Figure 8. Transient simulated waveforms of Second proposed design.

TABLE I. SIMULATIONS RESULTS OF D FLIP-FLOP CIRCUITS

circuits	Power(μw)	Delay(ps)	PDP(Je)
[2]	0.0779	3.1010	$2.415e^{-19}$
[2]	0.9134	3.4929	$31.9041e^{-19}$
[3]	4.8492	303.78	$14730e^{-19}$
First Proposed D flip-flop	0.117	2.3096	$2.7e^{-19}$
Second Proposed D flip-flop	0.0548	1.7342	$0.95e^{-19}$

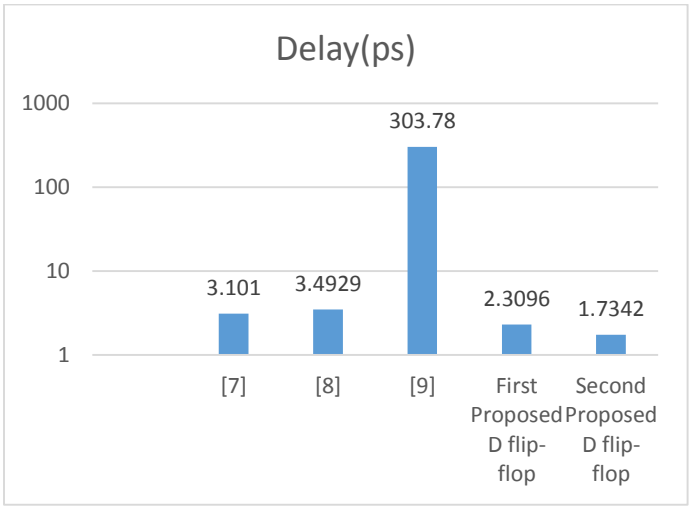

Figure 9. Delay analysis of designs.

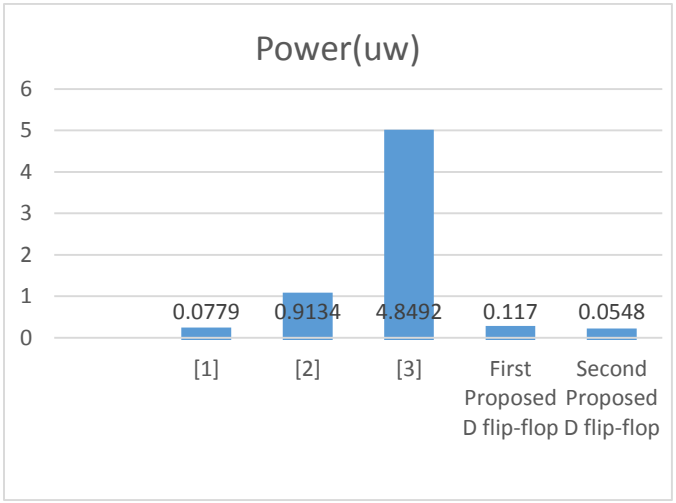

Figure 10. Power analysis of designs.

TABLE II. SIMULATIONS RESULTS OF PROPOSED CIRCUITS AT DIFFERENT OPERATING FREQUENCY

operating frequency	100MHZ		200MHZ		500MHZ		1GHZ	
	Power (μw)	Delay(ps)	Power (μw)	Delay(ps)	Power(μw)	Delay(ps)	Power (μw)	Delay (ps)
First proposed design	0.0098	2.53	0.026	2.48	0.055	2.39	0.11	2.3
Second proposed design	0.009	1.99	0.012	1.93	0.023	1.78	0.055	1.73

VI. CONCLUSION

In this paper two CNTFET based D flip-flop are presented in 32 nm CNTFET technology. Flip-flops are simulated in HSPICE with operating voltage of 1 volt and operating frequency at 1GHZ. The results shows the second design improved both delay and power compared with references 1,2and 3 by 44% and 29% respectively and the first design improved delay by 25% with slightly increase in power. Therefore the proposed D flip-flop is faster than the other circuits.

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